PATENT
Customer No. 22,852
Attorney Docket No. 06502.0366-00

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Guy L. STEELE, Jr.	)	Group Art Unit: 2193
	)	
Application No.: 10/035,584	)	Examiner: Do, Chat C.
	)	
Filed: December 28, 2001	)	
	)	
For: FLOATING POINT REMAINDER WITH EMBEDDED STATUS INFORMATION	)	Confirmation No.: 2869

Mail Stop Appeal Brief--Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL OF APPEAL BRIEF (37 C.F.R. 41.37)

Transmitted herewith is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on September 30, 2005.

This application is on behalf of

☐ Small Entity ☒ Large Entity

Pursuant to 37 C.F.R. 41.20(b)(2), the fee for filing the Appeal Brief is:

☐ $250.00 (Small Entity)

☒ $500.00 (Large Entity)

TOTAL FEE DUE:

Appeal Brief Fee	$ 500.00
Extension Fee (if any)	$1,590.00
Total Fee Due	$2,090.00

☒ Enclosed is a check for $2,090.00 to cover the above fees.

PETITION FOR EXTENSION. If any extension of time is necessary for the filing of this Appeal Brief, and such extension has not otherwise been requested, such an extension is hereby requested, and the Commissioner is authorized to charge necessary fees for such an extension to our Deposit Account No. 06-0916. A duplicate copy of this paper is enclosed for use in charging the deposit account.

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 7, 2006

By: _____
Nathan A. Sloan
Reg. No. 56,249

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:	)	
	)	
Guy L. STEELE, Jr.	)	Group Art Unit: 2124
	)	
Application No.: 10/035,584	)	Examiner: Chat C. Do
	)	
Filed: December 28, 2001	)	
	)	
For: FLOATING POINT REMAINDER WITH EMBEDDED STATUS INFORMATION	)	Confirmation No.: 2869

Attention: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF UNDER BOARD RULE § 41.37

In support of the Notice of Appeal filed September 30, 2005, and further to Board Rule 41.37, Appellant presents this brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 1.17(c).

This Appeal Brief is being filed concurrently with a Petition for an Extension of Time for four months and the appropriate fee.

This Appeal responds to the Notice of Panel Decision from Pre-Appeal Brief Review mailed on November 7, 2005 and the Final Office Action mailed on May 5, 2005, which rejected claims 1-37 under 35 U.S.C. § 103(a).

If any additional fees are required or if the enclosed payment is insufficient, Appellant requests that the required fees be charged to Deposit Account No. 06-0916.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

Sun Microsystems, Inc. is the real party in interest, as indicated by the assignment in its name, recorded at Reel 012440, Frame 0929 on December 28, 2001.

II. RELATED APPEALS AND INTERFERENCES

In accordance with 37 C.F.R. § 41.37(c)(1)(ii), Appellant advises the Board of Patent Appeals and Interferences (the "Board") of the following pending appeals, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the instant appeal:

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,595, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,579, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,587, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,647, in which an Appeal Brief was filed concurrently herewith.

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,580, in which an Appeal Brief was filed concurrently herewith.

III. STATUS OF CLAIMS

Claims 1-37 remain pending and under current examination.

Claims 1-37 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,995,991 to Huang et al. ("*Huang*") in view of U.S. Patent No. 5,065,352 to Nakano (*"Nakano"*). Appellant appeals this rejection of those claims.

Claims 1-37 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-37 of copending Application No. 10/035,580 in view of *Nakano*.

The attached Appendix contains a clean copy of the claims involved in the appeal, claims 1-37.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendments under 37 C.F.R. § 1.116 have been filed.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1, 14, and 26 of this application respectively recite a system, method, and computer-readable medium for providing a floating point remainder. *Specification*, p. 1, paragraph 02.

Digital electronic devices, such as digital computers, calculators and other devices, perform arithmetic calculations on values in integer, or "fixed point," format, in fractional, or "floating point" format, or both. *Specification*, p. 1, paragraph 03. Institute of Electrical and Electronic Engineers (IEEE) Standard 754, (hereinafter "IEEE Std.

754") published in 1985 and adopted by the American National Standards Institute (ANSI), defines several standard formats for expressing values in floating point format and a number of aspects regarding behavior of computation in connection therewith. *Id.*

In prior art devices that perform floating point computations, floating point status information generated by the computation is stored in a floating point status register. *Id.* at p. 7, paragraph 019. The status information is stored as conditions, represented by flags that are stored in the floating point status register. *Id.* at p. 7, paragraph 025.

However, the modes (*e.g.*, the rounding modes and traps enabled/disabled mode), flags (*e.g.*, flags representing the status information), and traps that are required to implement IEEE Std. 754 introduce implicit serialization issues. *Id.* at p. 8, paragraph 027. Implicit serialization is essentially the need for serial control of access (read/write) to and from globally used registers, such as a floating point status register. *Id.* The potential for implicit serialization makes the Standard difficult to implement coherently and efficiently in today's superscalar and parallel processing architectures without loss of performance. *Id.*

Moreover, the implicit side effects of a procedure that can change the flags or modes can make it very difficult for compilers to perform optimizations on floating point code. *Id.* at pp. 8-9, paragraph 028. As a result, compilers for most languages usually assume that every procedure call is an optimization barrier in order to be safe. *Id.* This unfortunately may lead to further loss of performance. *Id.*

The claimed invention addresses these and other problems of prior art floating point computational systems. *Id.* at p. 9, paragraph 032. Since the floating point status information comprises part of the floating point representation of the result, instead of

being separate and apart from the result as in prior art square root units, the implicit serialization that is required by maintaining the floating point status information separate and apart from the result may be obviated. *Id.* at p. 12, paragraph 044.

The invention, as recited by claim 1, relates to a system for providing a floating point remainder (*Id.* at p. 10, paragraph 033). The system may include an analyzer circuit (Fig. 1, 11A, 11B, 12A, 12B) configured to determine a first status of a first floating point operand (Fig. 1, 11A) and a second status of a second floating point operand (Fig. 1, 11B) based upon data within the first floating point operand and data within the second floating point operand respectively (*Id.* at p. 17, paragraph 055). The system may also include a results circuit (13, 14, 15) coupled to the analyzer circuit and configured to assert a resulting floating point operand containing the remainder of the first floating point operand and the second floating point operand and a resulting status embedded with the resulting floating point operand. *Id.*

The invention, as recited by claim 14, relates to a method for providing a floating point remainder. *Id.* at p. 10, paragraph 034. The method may include determining a first status of a first floating point operand (Fig. 1, 11A) and a second status of a second floating point operand (Fig. 1, 11B) based upon data within the first floating point operand and data within the second floating point operand respectively. *Id.* The method may also include asserting a resulting floating point operand containing the remainder of the first floating point operand and the second floating point operand and a resulting status embedded with the resulting floating point operand. *Id.*

The invention, as recited by claim 26, relates to a computer-readable medium on which is stored a set of instructions for providing a floating point remainder, which when

executed perform stages. *Id.* at p. 10, paragraph 035. The stages may include determining a first status of a first floating point operand (11A) and a second status of a second floating point operand (11B) based upon data within the first floating point operand and data within the second floating point operand respectively. *Id.* The stages may also include asserting a resulting floating point operand containing the remainder of the first floating point operand and the second floating point operand and a resulting status embedded with the resulting floating point operand. *Id.*

VI. GROUNDS OF REJECTION TO BE REVIEWED

A. Claims 1-37 have been finally rejected by the Examiner under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,995,991 to Huang et al. ("*Huang*") in view of U.S. Patent No. 5,065,352 to Nakano (*"Nakano"*). Appellant appeals this rejection of those claims.[1]

VII. ARGUMENT

A. Claims 1-37 patentably distinguish from *Huang* and *Nakano*

In view of the reasoning set forth below, Appellant respectfully requests the Board to reverse the Examiner's rejection of claims 1-37 under 35 U.S.C. § 103(a).

Several basic factual inquires must be made in order to determine the obviousness or non-obviousness of claims of a patent application under 35 U.S.C. § 103. These factual inquiries, set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), require the Examiner to:

(1) Determine the scope and content of the prior art;

[1] Pending withdrawal of the Examiner's rejection under 35 U.S.C. § 103(a), Appellant will obviate the double patenting rejection as appropriate. Appellant does not request review of the double patenting rejection.

> (2) Ascertain the differences between the prior art and the claims in issue;
> (3) Resolve the level of ordinary skill in the pertinent art; and
> (4) Evaluate evidence of secondary considerations.

The obviousness or nonobviousness of the claimed invention is then evaluated in view of the results of these inquiries. *Graham*, 383 U.S. at 17-18, 148 USPQ 467.

Thus, in order to carry the initial burden of establishing a *prima facie* case of obviousness that satisfies the *Graham* standard, the Examiner must show that the prior art reference teaches or suggests all the claim elements. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). The Examiner must also show that there is some suggestion or motivation, either in the reference or in the knowledge generally available to one of ordinary skill in the art, to modify the reference. *In re Rouffet*, 149 F.3d 1350, 47 USPQ2d 1453 (Fed. Cir. 1998). "Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference." *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1316-17 (Fed. Cir. 1998) (citations omitted). In addition, the suggestion or motivation "must be found in the prior art reference, not in the Applicant's disclosure." *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991).

B. Neither *Huang* nor *Nakano* teaches or suggests all of Appellant's claim elements.

Neither *Huang* nor *Nakano*, taken alone or in combination, teaches or suggests each and every element of Appellant's claimed invention. Independent claim 1 calls for a combination including, for example,

> an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively

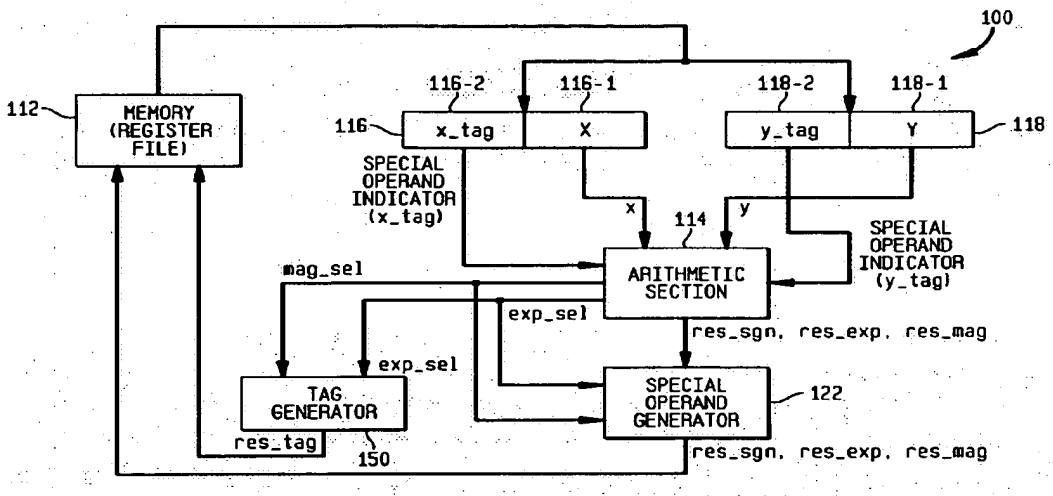
(emphasis added). *Huang* fails to teach or suggest these elements.

The Examiner asserts that *Huang's* elements 116-2 and 118-2 in Figure 4 constitute the claimed analyzer circuit.[2] *Office Action mailed May 5, 2005* at p. 2. The Examiner also asserts that "the floating-point operand with special tag is considered as a single unit/operand," and concludes that "[t]hus, each floating-point operand in Huang et al.'s reference including a tag unit and a value unit wherein the tag unit is embedded within the operand." *Id.* at p. 9. These assertions are incorrect. *Huang's* "tag value" (alleged status), is not "data within the first floating point operand and data within the second floating point operand," as recited by claim 1 (emphasis added).

Huang teaches "each portion of the registers 116 and 118 has an operand value storage portion 116-1 and 118-1 and a tag value storage portion 116-2 and 118-2" (emphasis added, *Huang*, col. 6, line 66 through col. 7, line 2). *Huang's* register is not an "operand," as recited by claim 1. As illustrated in FIG. 4 of *Huang*, which Appellant reproduces below, register 116 contains a separate operand value storage portion, 116-1, and a separate tag value storage portion for the x_tag 116-2 (*Huang*, col. 6, line 66 through col. 7, line 2; Fig. 4).

2 The Examiner also references *Huang's* elements 24 and 26 in Fig. 1. However, Fig. 1 of *Huang* is directed to prior art. If the Examiner continues to rely on the combination of Fig. 1 and Fig. 4 of *Huang*, the rejection should be under 35 U.S.C. § 103(a) and the Examiner must overcome the presumption that Fig. 4 of *Huang* teaches away from the prior art discussed in Fig. 1. *See Huang*, col. 5, lines 3-7.

FIG. 4



Thus, *Huang's* tag value stored in 116-2 is clearly not "data within" *Huang's* operand value stored in 116-1. Therefore, *Huang* does not teach or suggest at least a system to "determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand," as recited by claim 1 (emphasis added).

Moreover, independent claim 1 also recites a combination including, for example, "a resulting status embedded within the resulting ... operand," (emphasis added). *Huang* does not teach or suggest at least this additional element.

The Examiner asserts that the output of *Huang's* tag generator 150 (FIG. 4) constitutes the claimed "resulting status embedded within the resulting floating point operand." *Office Action mailed May 5, 2005* at p. 3. However, as illustrated in FIG. 4 of

Huang, the output of *Huang's* tag generator 150 (alleged status) is separate from the output of the special operand generator 122. These results are stored and loaded separately into the tag value portion 116-2 and operand value portion 116-1, as discussed above. Such teachings by *Huang* do not constitute a teaching or suggestion of "a resulting status embedded within the resulting floating point operand," as recited by claim 1 (emphasis added).

Structures such as those taught by *Huang* were acknowledged in the Background section of Appellant's specification, which states "conditions are typically represented by flags that are stored in the floating point status register" (paragraph 025). Claim 1 specifically distinguishes over such structures, calling for determining a first and second status of a first and second operand "based upon data within the first floating point operand and data within the second floating point operand" (emphasis added). Claim 1 also distinguishes over such structures by calling for "a resulting status embedded within the resulting floating point operand" (emphasis added). *See also* Appellant's Figs. 2, 4a, 4b, and 4c.

Nakano fails to cure the deficiencies of *Huang*, nor does the Examiner rely on *Nakano* for such teachings. The Examiner relies on *Nakano* for allegedly teaching "a remainder of two operands division." *Office Action mailed May 5, 2005* at p. 3. Even assuming this allegation is true, *Nakano* fails to teach or suggest "determining a first and second status of a first and second operand "based upon data within the first floating point operand and data within the second floating point operand," as recited by claim 1 (emphasis added). *Nakano* also fails to teach or suggest "a resulting status

embedded within the resulting floating point operand," as recited by claim 1 (emphasis added).

Because neither *Huang* nor *Nakano* teaches or suggests each and every element recited by claim 1, no *prima facie* case of obviousness has been established for this claim. Independent claims 14 and 26, although of different scope, recite elements similar to claim 1. Claims 2-13, 15-25, and 27-37 depend from independent claims 1, 14, and 26, and therefore include all of the elements recited therein. Accordingly, for at least the reasons discussed above with respect to claim 1, no *prima facie* case of obviousness has been established with respect to claims 2-37. Appellant requests that the Board overturn the Examiner's rejection of claims 1-37.

VIII. CONCLUSION

For the reasons given above, the Examiner has not established a *prima facie* case of obviousness with respect to the appealed claims. Accordingly, pending claims 1-37 are allowable and reversal of the Examiner's rejections are respectfully requested.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 which are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: April 7, 2006

By: _____
Nathan A. Sloan
Reg. No. 56,249

IX. Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

1. A system for providing a floating point remainder, comprising:

an analyzer circuit configured to determine a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

a results circuit coupled to the analyzer circuit and configured to assert a resulting floating point operand containing the remainder of the first floating point operand and the second floating point operand and a resulting status embedded with the resulting floating point operand.

2. The system for providing a floating point remainder of claim 1, wherein the analyzer circuit further comprises:

a first operand buffer configured to store the first floating point operand;

a second operand buffer configured to store the second floating point operand;

a first operand analysis circuit coupled to the first operand buffer, the first operand analysis circuit configured to generate a first characteristic signal having information relating to the first status; and

a second operand analysis circuit coupled to the second operand buffer, the second operand analysis circuit configured to generate a second characteristic signal having information relating to the second status.

3. The system for providing a floating point remainder of claim 2, wherein the first status and the second status are determined without regard to memory storage external to the first operand buffer and the second operand buffer.

4. The system for providing a floating point remainder of claim 3, wherein the memory storage external to the first operand buffer and the second operand buffer is a floating point status register.

5. The system for providing a floating point remainder of claim 1, wherein the results circuit further comprises:

a remainder circuit coupled to the analyzer circuit, the remainder circuit configured to produce the remainder of the first floating point operand and the second floating point operand;

a remainder logic circuit coupled to the analyzer circuit and configured to produce the resulting status based upon the first status and the second status; and

a result assembler coupled to the remainder circuit and the remainder logic circuit, the result assembler configured to assert the resulting floating point operand and embed the resulting status within the resulting floating point operand.

6. The system for providing a floating point remainder of claim 5, wherein the remainder logic circuit is organized according to a structure of a decision table.

7. The system for providing a floating point remainder of claim 1, wherein the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, a division by zero status, an infinity status, and an inexact status.

8. The system for providing a floating point remainder of claim 7, wherein the overflow status represents one in a group of a plus overflow (+OV) status and a minus overflow (-OV) status.

9. The system for providing a floating point remainder of claim 7, wherein the overflow status is represented as a predetermined non-infinity numerical value.

10. The system for providing a floating point remainder of claim 7, wherein the underflow status represents one in a group of a plus underflow (+UN) status and a minus underflow (-UN) status.

11. The system for providing a floating point remainder of claim 7, wherein the underflow status is represented as a predetermined non-zero numerical value.

12. The system for providing a floating point remainder of claim 7, wherein the invalid status represents a not-a-number (NaN) status due to an invalid operation.

13. The system for providing a floating point remainder of claim 7, wherein the infinity status represents one in a group of a positive infinity status and a negative infinity status.

14. A method for providing a floating point remainder, comprising:

determining a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

asserting a resulting floating point operand containing the remainder of the first floating point operand and the second floating point operand and a resulting status embedded with the resulting floating point operand.

15. The method for providing a floating point remainder of claim 14, wherein the determining stage further comprises:

storing the first floating point operand in a first operand buffer;

storing the second floating point operand in a second operand buffer;

generating a first characteristic signal representative of the first status; and

generating a second characteristic signal representative of the second status.

16. The method for providing a floating point remainder of claim 15, wherein the first characteristic signal and the second characteristic signal are generated without regard to memory storage external to the first operand buffer and the second operand buffer.

17. The method for providing a floating point remainder of claim 16, wherein the memory storage external to the first operand buffer and the second operand buffer is a floating point status register.

18. The method for providing a floating point remainder of claim 14, wherein the asserting stage further comprises:

producing the remainder of the first floating point operand and the second floating point operand; and

asserting the resulting floating point operand.

19. The method for providing a floating point remainder of claim 14, wherein the first status, the second status, and the resulting status are each one of the following: an invalid operation status, an overflow status, an underflow status, a division by zero status, an infinity status, and an inexact status.

20. The method for providing a floating point remainder of claim 19, wherein the overflow status represents one in a group of a plus overflow (+OV) status and a minus overflow (-OV) status.

21. The method for providing a floating point remainder of claim 20, wherein the overflow status is represented as a predetermined non-infinity numerical value.

22. The method for providing a floating point remainder of claim 19, wherein the underflow status represents one in a group of a plus underflow (+UN) status and a minus underflow (-UN) status.

23. The method for providing a floating point remainder of claim 22, wherein the underflow status is represented as a predetermined non-zero numerical value.

24. The method for providing a floating point remainder of claim 19, wherein the invalid status represents a not-a-number (NaN) status due to an invalid operation.

25. The method for providing a floating point remainder of claim 19, wherein the infinity status represents one in a group of a positive infinity status and a negative infinity status.

26. A computer-readable medium on which is stored a set of instructions for providing a floating point remainder, which when executed perform stages comprising:

determining a first status of a first floating point operand and a second status of a second floating point operand based upon data within the first floating point operand and data within the second floating point operand respectively; and

asserting a resulting floating point operand containing the remainder of the first floating point operand and the second floating point operand and a resulting status embedded with the resulting floating point operand.

27. The computer-readable medium of claim 26, wherein the determining stage further comprises:

storing the first floating point operand in a first operand buffer;

storing the second floating point operand in a second operand buffer;

generating a first characteristic signal representative of the first status; and

generating a second characteristic signal representative of the second status.

28. The computer-readable medium of claim 27, wherein the first characteristic signal and the second characteristic signal are generated without regard to memory storage external to the first operand buffer and the second operand buffer.

29. The computer-readable medium of claim 28, wherein the memory storage external to the first operand buffer and the second operand buffer is a floating point status register.

30. The computer-readable medium of claim 26, wherein the asserting stage further comprises:

producing the remainder of the first floating point operand and the second floating point operand; and

asserting the resulting floating point operand.

31. The computer-readable medium of claim 26, wherein the first status, the second status, and the resulting status are each one of the following: an invalid

operation status, an overflow status, an underflow status, a division by zero status, an infinity status, and an inexact status.

32. The computer-readable medium of claim 31, wherein the overflow status represents one in a group of a plus overflow (+OV) status and a minus overflow (-OV) status.

33. The computer-readable medium of claim 32, wherein the overflow status is represented as a predetermined non-infinity numerical value.

34. The computer-readable medium of claim 31, wherein the underflow status represents one in a group of a plus underflow (+UN) status and a minus underflow (-UN) status.

35. The computer-readable medium of claim 34, wherein the underflow status is represented as a predetermined non-zero numerical value.

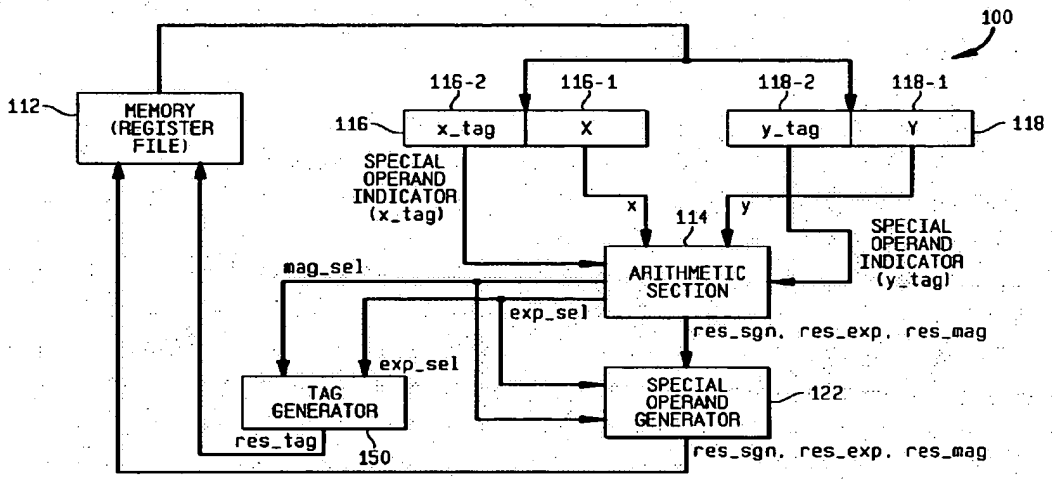
36. The computer-readable medium of claim 31, wherein the invalid status represents a not-a-number (NaN) status due to an invalid operation.

37. The computer-readable medium of claim 31, wherein the infinity status represents one in a group of a positive infinity status and a negative infinity status.

X. Evidence Appendix to Appeal Brief Under Rule 41.37(c)(1)(ix)

Appellant relies on Fig. 4 of *Huang*, which is reproduced below.

FIG. 4



XI. Related Proceedings Appendix to Appeal Brief Under Rule 41.37(c)(1)(x)

The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,747, in which an Appeal Brief was filed concurrently herewith.

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The Appeal of In re Application of Guy STEELE, Jr., U.S. Patent Application No. 10/035,580, in which an Appeal Brief was filed on concurrently herewith.